IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Appl. No.	:	10/681,068	Confirmation No. : 8619
Appellant	:	Andrew S. Hildebrant, et al.	
Filed	:	October 7, 2003	
TC/A.U.	:	3714	
Examiner	:	Frank M. Leiva	
Docket No.	:	10030549-1	

Mail Stop Appeal Brief – Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

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APPEAL BRIEF

Dear Sir:

This Appeal Brief is submitted in response to the Examiner's Office Action mailed October 28, 2008. Of note, this is the third consecutive Appeal Brief filed by appellants. Each of the past two Appeal Briefs has been followed by an attempt to re-open prosecution.

Appellants have filed a new Notice of Appeal on today's date - January 28, 2009.

Real Party in Interest

The real party in interest is Verigy (Singapore) Pte. Ltd., a Singapore limited liability company.

Related Appeals and Interferences

The rejections of the claims in United States patent application no. 10/666,024 have been appealed to the Board of Patent Appeals and Interferences. The decision on this appeal, when made, could be relevant to the appeal of the rejections of the claims in the instant application.

Status of Claims

Claims 1-17 are pending, all of which stand rejected. The rejections of claims 1-17 are appealed.

A copy of the claims is attached as a Claims Appendix to this Appeal Brief.

Status of Amendments

No amendments were made to the claims subsequent to final rejection. All amendments have been entered.

Summary of Claimed Subject Matter

In a first embodiment (claim 1) a machine-executable method comprises 1) reading a test file having a plurality of test vectors (p. 5, lines 10-18; FIG. 2, 200), 2) determining a required memory needed to execute the plurality of test vectors (p. 5, line 19 - p. 6, line 13; FIG. 2, 205), and 3) using the required memory to estimate a cost to execute the test vectors (p. 6, lines 14-20; FIG. 2, 210).

In a second embodiment (claim 8), a system (p. 4, lines 3-4; FIG. 1, 100) comprises 1) logic (FIG. 1, 102) to read a test file having a plurality of test vectors (p. 4, lines 5-6; p. 5, lines 10-18) and to determine a required memory needed to execute the plurality of test vectors (p. 4, lines 5-7; p. 5, line 19 - p. 6, line 13), and 2) a billing predictor (p. 4, lines 8-14; p. 6, lines 14-20; FIG. 1, 104), communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

In a third embodiment (claim 13), one or more machine-readable mediums have sequences of instructions stored thereon (p. 9, lines 5-10). When executed by a machine, the sequences of instructions cause the machine to perform the following actions: 1) read a test file having a plurality of test vectors (p. 5, lines 10-18; FIG. 2, 200); 2) determine a required memory needed to execute the plurality of test vectors (p. 5, line 19 - p. 6, line 13; FIG. 2, 205); and 3) use the required memory to estimate a cost to execute the test vectors (p. 6, lines 14-20; FIG. 2, 210).

Ground of Rejection to be Reviewed on Appeal

Whether claims 1-17 should be rejected under 35 USC 103(a) as being unpatentable over Park et al. (US 7,185,295 B2) in view of Boateng (US 2002/0184587 A1) and Ohara et al. (US 2002/0143418 A1).

Argument

Claims 1-17 should not be rejected under 35 USC 103(a) as being unpatentable over Park et al. (US 7,185,295 B2; hereinafter "Park") in view of Boateng (US 2002/0184587 A1) and Ohara et al. (US 2002/0143418 A1; hereinafter "Ohara").

With respect to claim 1, the Examiner asserts that Park teaches the steps of "reading a test file having a plurality of test vectors" and "determining a required memory needed to execute the plurality of test vectors" in col. 12, lines 9-16, and col. 17, lines 1-5.

Col. 12, lines 9-16, of Park state:

> A device user designates an initial value set for various kinds of variables, user-designated variables, and relevant variables using the GUI menu items (step 110). In the step 110, signals are allocated to pins of the third and fourth connectors C3 and C4 of the interface means 32 of FIG. 4. A size of each of the frame buffers of the interface means 32 is determined, and a size of the chunk memory for a display operation is determined.

Col. 17, lines 1-5, of Park state:

> In case that ***the input file of or the test vector file*** of the target 34 is already compressed and stored in the hard disk 33, an access time of the hard disk 22 to read and store files of the same size can be as reduced as a data compression ratio.
>
> (emphasis added).

Appellants assert that nothing in the above disclosure (or in Park's disclosure, as a whole) indicates that a determination is made regarding the required memory needed to execute a plurality of test vectors.

As noted above, Park indicates that the sizes of "frame buffer" and a "chunk memory" are determined in a step 110. Park further indicates that, after these sizes are determined,

> . . .the device user sets an operation mode of the interface means 32 using menu items of the GUI (step 120). The operation mode includes a verifying mode and a testing mode.. . .In the test mode, it is set whether to use the interface means 32 as a pattern generator or/and a logic analyzer, and an operation is performed that inputs or outputs data of ***one frame unit*** to the target 34 at a high speed.
>
> Park, col. 12, lines 30-41 (emphasis added).

With respect to how the frame buffer is used in the test mode, Park further indicates:

> FIGS. 17a and 17b are a flow chart illustrating a chip testing method according to the preferred embodiment of the present invention and shows that the target 34 includes the hardware and software models embodied in the same method as that of FIG. 14. An operation of the steps 800 to 840 is equal to that of the steps 300 to 340 of FIG. 14. However, in the step 810, the frame buffer is designated to an initial value, ***according to a size of the test vector***, a size of the frame buffer region of the main memory 18 and a size of the frame buffer region of the memory 40 of the interface means 32. When a size of the memory 40 of the interface means 32 is relatively small, either a memory board having the same memories as the memories M1 to M4 of the memory 40 of the interface means 32 or the memory 40 of the neighboring interface means 32 that is not being used may be connected to the first connector C1. In the step 820, an operation mode of the interface means 32 is set to the pattern generator and/or the logic analyzer.
>
> After storing all of the input data constituting the test vector in the memory 40 of the interface means 32, data stored in the memory 40 of the interface means 32 are applied to the target 34, and data outputted from the target 34 are compared with expected data (step 850). That is, in case of testing a chip, after storing all of the input data constituting test vector in the memory of the interface means 32, data are transmitted between the interface means 32 and the target 34 at the same speed of an operation speed of the chip that is a target. Therefore, a test can be performed even when an operation speed of the chip is high.
>
> Park, col. 21, line 43 - col. 22, line 4 (emphasis added).

From the above disclosure of Park, appellants believe it is clear that Park's frame buffer holds, or is sized to hold, one test vector at a time. As a result, Park never performs the step of "determining a required memory needed to execute ***the***

plurality of test vectors". Furthermore, nothing disclosed by Park implies that one should configure a frame buffer to store multiple test vectors, or that one should determine the required memory needed to store "the input file or the test vector file" mentioned in col. 17, line 1, quoted *supra*.

For the above reasons, appellants believe it is clear that Park fails to teach the second step of their claim 1. Boateng and Ohara also fail to teach this step. As a result, the Examiner has not made a prima facie case for rejecting claim 1.

Further, with respect to claim 1, the Examiner asserts that Boateng, in par. [0006], discloses the importance of determining memory size due to the high cost of memory. Appellants disagree. Boateng generally discloses that 1) "The cost of applying [a] large set of test vectors is high since the cost of test equipment is related to its memory capacity", and 2) "Re-loading of the test equipment [memory] during testing significantly prolongs the test application time". Appellants assert that these are merely statements of generally known 'truths', which truths serve as a motivation for Boateng's "Apparatus and Method for Test-Stimuli Compaction" (see, Boateng's Title). Because Park's "frame buffer" only holds a single test vector, appellants do not see any reason why one of ordinary skill in the art, at the time of appellants' invention, would have been motivated to modify Park's disclosed methods and apparatus in light of Boateng's disclosure. Furthermore, Park already indicates that:

> . . .However, there is a limitation to expanding a memory capacity of the interface means 32, and thus it is preferable to use a method of compressing and then storing data in the interface means 32. In other words, ***the test vector stored in the hard disk 22 is compressed using a software program and then stored in the frame buffer region of the main memory 18***. . .
>
> Col. 14, lines 23-29 (emphasis added).

Given this, appellants fail to see how one of ordinary skill in the art would have modified Park's disclosure to introduce any functionality not already provided by Park's methods and apparatus.

With respect to claim 1's step of "using the required memory to estimate a cost to execute the test vectors", the Examiner admits that Park and Boateng fail to disclose this step. However, the Examiner notes that:

> . . .Ohara on the other hand teaches an automated method for calculating project costs which when applied to the Williams invention would use the calculated required memory to estimate a cost to execute the test vectors.
>
> 10/28/2008 Office Action, p. 4, sec. 8.

Although Ohara discloses a "product cost variance analysis system and control method" (*see*, e.g., Title; Abstract), appellants cannot find any mention by Ohara that its disclosed systems and methods should be applied to "test vectors" or memories. Nonetheless, the Examiner asserts that it would be obvious to combine Ohara's teachings with Park's and Boateng's because Ohara's method for calculating project costs could be used on Park's calculation of a "required memory" to estimate the cost to execute a plurality of test vectors. Yet, as already discussed, Parks never discloses (or even implies) that the "required memory needed to execute the plurality of test vectors" should be calculated (or determined). This being the case, appellants cannot think of any reason why one of ordinary skill in the art would be motivated to combine Ohara's teachings with those of Park and Boateng.

For the above reasons, claim 1 is believed to be allowable over the combined teachings of Park, Boateng and Ohara.

Claims 2-7 are believed to be allowable, at least, because they depend from claim 1.

Claims 8 and 13 are believed to be allowable, at least, for reasons similar to why claim 1 is believed to be allowable.

Claims 9-12 and 14-17 are believed to be allowable, at least, because they depend from claim 8 or 13.

Conclusion

In summary, the art of record does not teach nor suggest the subject matter of appellant's claims 1-17. These claims are therefore believed to be allowable.

Respectfully submitted,
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Claims Appendix

1. A machine-executable method comprising:

reading a test file having a plurality of test vectors;

determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

2. The method of claim 1, further comprising receiving a billing scheme and wherein using the required memory to estimate a cost includes using the billing scheme to estimate the cost to execute the test vectors.

3. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

4. The method of claim 1, wherein determining a required memory comprises determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

5. The method of claim 1, wherein determining a required memory comprises counting the number of test vectors for each of one or more tests in the test file.

6. The method of claim 1, wherein determining a required memory comprises:

determining a first memory requirement needed for a first pin of a tester to execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

7. The method of claim 6, further comprising for each additional test in the test file:

for each pin of the tester, determining a third memory requirement for the pin to execute the test vectors for the additional test; and setting the required memory equal to the third memory requirement if the third memory requirement is greater than the required memory.

8. A system comprising:

logic to read a test file having a plurality of test vectors and to determine a required memory needed to execute the plurality of test vectors; and

a billing predictor, communicatively coupled to the logic, to use the required memory to estimate a cost to execute the test vectors.

9. The system of claim 8, further comprising a user interface to display the cost to a user.

10. The system of claim 8, wherein the tester includes a plurality of boards, and wherein the logic is to determine a required memory needed for each board of a tester to execute the test vectors for the board.

11. The system of claim 8, wherein the tester includes a plurality of boards, each board including a plurality of pins; and wherein the logic is to determine a required memory needed for each pin to execute the test vectors for the pin.

12. The system of claim 8, wherein the logic is to determine the required memory by counting the number of test vectors for each test in the test file.

13. One or more machine-readable mediums having stored thereon sequences of instructions, which, when executed by a machine, cause the machine to perform the actions:

reading a test file having a plurality of test vectors;

determining a required memory needed to execute the plurality of test vectors; and

using the required memory to estimate a cost to execute the test vectors.

14. The machine-readable mediums of claim 13, further comprising instructions, which when executed by the machine, cause the machine to perform the actions of receiving a billing scheme; and wherein the instructions for using the required memory to estimate a cost include instructions, which when executed by the machine, cause the machine to perform the actions of using the billing scheme to estimate the cost to execute the test vectors.

15. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions of determining a required memory needed for each of a plurality of boards of a tester to execute the test vectors for the board.

16. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions of determining a required memory needed for each of a plurality of pins of a tester to execute the test vectors for the pin.

17. The machine-readable mediums of claim 13, wherein the instructions for determining a required memory comprise instructions, which when executed by the machine, cause the machine to perform the actions:

determining a first memory requirement needed for a first pin of a tester to

execute the test vectors for a first test in the test file;

setting the required memory equal to the first memory requirement; and

for each additional pin of the tester,

determining a second memory requirement needed for the additional pin to execute the test vectors for the first test; and

if the second memory requirement is greater than the first memory requirement, setting the required memory equal to the second memory requirement.

Evidence Appendix

None.

Related Proceedings Appendix

None.